Digital Pulse Modulation Amplifier (PMA) topologies based on PEDEC Control **4942 (O2)**

Karsten Nielsen, *Bang & Olufsen A/S, Struer, Denmark*

Presented at the 106th Convention 1999 May 8–11 Munich, Germany

AES

AN AUDIO ENGINEERING SOCIETY PREPRINT

Digital Pulse Modulation Amplifier (PMA) systems based on PEDEC control

Karsten Nielsen
M.Sc.E.E, Ph.D

Bang & Olufsen A/S, Denmark
&
IAE, Technical University of Denmark

E-mail: kst@bang-olufsen.dk

Abstract

The paper extends previous research and presents three Pulse Modulation power Amplifier (PMA) topologies based on Pulse Edge Delay Error Correction (PEDEC). The proposed topologies are believed to be the first implemented digital PMA systems that maintains the digital modulator performance throughout the subsequent power conversion by effective error correction. The results are very encuraging.

1. Introduction

The digital Pulse Modulation Amplifier (PMA) topology, also known as the digital power amplifier, is appealing from a theoretical point of view in applications where the source material is digital. No analog modulator or carrier generator is needed and the digital modulator can provide a very consistent, good performance. As clarified in earlier papers on the subject within the last decade, the non-linearity of the switching power stage presents a significant impediment to maintain the modulator performance throughout the subsequent power conversion by a switching power stage.

Undoubtedly, a switching power amplification stage can be tuned to high linearity, much better performance than that of linear output stages. However, this is a complex task that requires e.g. perfect control over the switching transitions, power supply stabilization., i.e. a low noise switch mode supply is needed. Furthermore, filter linearity is a concern. The filter design gets more complicated and requires much attention. Linear core-materials or air cored inductors are necessary without error correction. Obviously, direct digital PCM-PWM based power conversion will never be very *elegant* or *practical*. A control system is desirable to eliminate this dependency of the many uncontrollable parameters relating to semiconductor physics, magnetics etc, such that the performance is controlled by a few e.g. passive components. The control system should be able to correct *effectively* for power stage errors by *simple* means. This will lead to improved and much more consistent performance than can be achieved with any power output stage operating open-loop. The research activity to correct for these errors has been very limited, and to the best of the authors knowledge no high performance amplifier system with a reasonable power handling capability exists to date, mainly due to these limitations. One of the reasons is that feedback would require an A/D converter in the feedback path.

This paper investigates solutions to this fundamental problem that has persisted in digital PMA systems. A novel pulse referenced control method was proposed in an earlier paper [8] – **Pulse Edge Delay Error Correction (PEDEC).** A extended PEDEC concept will be introduced as a general method for enhanced power amplification of a pulse modulated signal. Following, the method is applied to digital PMA systems, and three general digital PMA topologies are proposed in the paper. The topologies are investigated by simulation and by practical evaluation.

2. The Digital Pulse Modulation Amplifier (PMA)

PEDEC will be investigated in combination with digital PWM. Various methods can be used to implement the modulator [1] - [5], [11], [12]. Fig. 1

shows an enhanced digital PWM modulator topology which has been widely used in previous litterature using various methods of precompensation. The analysis of distortion and general spectral characteristics of digital modulators in previous litterature has illustrated, how e.g. LPWM [2] can provide a very good approximation to natural sampling. Fig. 2 shows a simulation from [12], where the digital pulse modulator output with a 1KHz input at 0.1 modulation index. The noise shaper is 5. order FIR filter with a stopband attenuation of –50dB [12]. The modulator maintains the input resolution and the output is virtually distortion free. Only at high frequencies and with deep modulation the distortion is noticeable with a maximum of 0.009% at modulation index M=0.9 and a 6.6 KHz input tone. This level of linearity performance cannot be reproduced by a simple power stage without compensation for the errors that are introduced in the power conversion process [12], [16].

3. Pulse Edge Delay Error Correction

Pulse Edge Delay Error Correction (PEDEC) [8] is a general pulse referenced control method for enhanced power amplification of a pulse modulated signal. Applications are digital PMAs and general DC-DC and DC-AC power amplification where accurate and distortion free power amplification of a pulse modulated signal is required. The basic idea is to introduce a correction unit in-between the (ideal) pulse modulator and the switching power amplification stage. The general block diagram for a PEDEC controller is shown in Fig. 3. The modulator output is feed to a correction unit that provides compensation by intelligently delaying the individual pulse edges, controlled by an input control signal. The re-timing is controlled to have a " pre-distorting " effect, such that the resulting switching power stage output is free from distortion, noise or any other undesired contribution. The validity of this approach are two fundamental facts:

- Digital modulators will generate a high quality output. The pulse-modulated signal may as such be used as reference for error correction.
- *All* power stage error sources can be corrected by intelligent pulse re-timing, *and* all error sources only need minor pulse edge re-timing for perfect elimination.

The general PEDEC controller can be viewed as a dual reference input pulse reference feedback control system comprising:

- The PEDEC unit with means to control the delays of the individual edges on the reference input v_r, based on a control input v_e. The PEDEC unit output is the corrected or "pre-distorted" signal.
- A state feedback block A that includes compensation from the power stage block.

- An optional reference shaping block R that serves to optimize the error estimation.
- A subtraction unit to generate error information.
- A compensator C to shape the error that feeds the PEDEC unit (v_e).

The following sections will introduce a range of new parameters, defined in Table 1, in order to provide a coherent analysis.

Parameter	Description
v_e	Control error signal to PEDEC unit
v_r ($\tilde{v}_r$)	Reference signal (pulse modulator output). (~) indicates the average or low frequency part of the signal.
v_c ($\tilde{v}_c$)	Pulse edge delayed PEDEC unit output voltage. (~) indicates the average or low-frequency component of the modulated signal.
t_s	Switching period.
t_0	Central PEDEC unit parameter, corresponding to the maximal effective pulse width change.
$t_l, \hat{t}_l$	Leading edge transition time before and after (^) correction
$t_t, \hat{t}_t$	Leading edge transition time before and after (^) correction
$t_w, \hat{t}_w$	Pulse width before and after (^) correction: $t_w = t_t - t_l$
V_R	Pulse modulator output voltage level.
V_I	Limited integrator output pulse voltage level.
V_C	PEDEC unit output pulse level.
V_{CC}	Power rail voltage level.

Table 1 Definition of fundamental PEDEC parameters.

3.1 Control function specification

Let the control error signal to the PEDEC unit realize a controlled function on the pulse edges, such that the effective change in pulse width Δt_w at the end of the switching cycle is proportional to the control signal v_e:

$$\Delta t_w = k_w \cdot v_e \tag{1}$$

Correspondingly:

$$\frac{dt_w}{dv_e} = k_w \tag{2}$$

The relationship between an increment in pulse width Δt_w and the corresponding change in the average of the PEDEC output $\Delta \tilde{v}_c$ can be

established by averaging within a single switching cycle. Assuming for simplicity here, that the PEDEC output pulse amplitude is unity:

$$\Delta\tilde{v}_c = \frac{1}{t_s}\left(\int_0^{d\cdot t_s+\Delta t_w} 1\cdot dt + \int_{d\cdot t_s+\Delta t_w}^{t_s} (-1)\cdot dt \right) = \frac{2}{t_s}\Delta t_w \tag{3}$$

Where d is the duty-cycle within the present switching cycle. Hence:

$$\frac{d\tilde{v}_c}{dt_w} = \frac{2}{t_s} \tag{4}$$

The fundamental linear PEDEC control function arrives by combining (2) and (4):

$$k_{PEDEC} = \frac{d\tilde{v}_c}{dv_e} = \frac{2k_w}{t_s} \tag{5}$$

Clearly, the control function is linear. This simplifies PEDEC controller design, since the whole machinery of linear control system design and verification can be fully utilized. Obviously, other control functions (e.g. non-linear functions) could be interesting alternatives for PEDEC. This could be a subject for future research.

3.2 Realizing the control function

This section proposes a simple approach to implement the double sided PEDEC unit, which implements the above specified control function. The method is shown in Fig. 4. The pulse delay correction is realized by a limited integration of the incoming (ideal) pulse waveform generating the signal v_i, and comparing this modified reference with the control signal v_e. The effective pulse width change, Δt_w, will be the difference between the leading edge delay and the trailing edge delay. From Fig. 4 it is obvious that $v_e > 0$ will increase the pulse width, whereas $v_e < 0$ will lead to a negative Δt_w. The following relations are obtained from the proposed double edge correction scheme in Fig. 4:

$$\hat{t}_l = t_l + \frac{t_0}{2} + t_0\frac{v_e}{2V_I}, \quad \hat{t}_t = t_t + \frac{t_0}{2} - t_0\frac{v_e}{2V_I} \tag{6}$$

Δt_w is derived:

$$\hat{t}_w = \hat{t}_t - \hat{t}_l = t_w - t_0 \frac{v_e}{V_l} \quad \Rightarrow$$

$$\Delta t_w = \hat{t}_t - \hat{t}_l = \begin{cases} t_0 & (v_e > V_l) \\ t_0 \frac{v_e}{V_l} & (-V_l \le v_e \le V_l) \\ -t_0 & (v_e < V_l) \end{cases} \tag{7}$$

In other words k_w as defined in (1) is:

$$k_w = \frac{dt_w}{dv_e} = \frac{t_0}{V_l} \tag{8}$$

From Fig. 4, the following relationship between and increment in pulse width dt_w and $\tilde{v}_c$ is established:

$$\frac{d\tilde{v}_c}{dt_w} = \frac{2V_C}{t_s} \tag{9}$$

Combining (8) and (9):

$$k_{PEDEC} = \frac{d\tilde{v}_c}{dv_e} = \frac{2V_C}{V_l} \frac{t_0}{t_s} \tag{10}$$

Assuming without loss of generality that the pulse amplitudes are adjusted to $V_C = V_l$, the following expression of the equivalent PEDEC unit control gain emerge:

$$\boxed{k_{PEDEC} = \frac{2t_0}{t_s}} \tag{11}$$

4. Applying PEDEC to Digital PMA systems

PEDEC can be considered as a general control method for improved power amplification of a pulse-modulated signal. The generality of the principle means that it can be used advantageously in combination with a range of different control structures. There are some significant differences between linear controller design for analog PMAs [12], and linear controller design using PEDEC. First of all, the loop in the PEDEC based system does not enclose a modulator. The equivalent linear gain of the power is the pulse amplification factor:

$$K_P = \frac{V_{CC}}{V_R} \tag{12}$$

Another significant difference is the effects of v_p, i.e. the tradeoffs between bandwidth and carrier frequency is different. An interesting property of PEDEC control is that the noise from v_p may be nearly eliminated by proper reference shaping (R), such that the noise on the control signal v_e is also minimized. PEDEC also differs from conventional control systems by the limited correction range of the PEDEC unit. This has significant importance in terms of gain control in that the range of system gain adjustment will be limited. Furthermore, the switching frequency has determining influence on the control system. This has to be taken into account during controller design.

4.1 Defining control structures

Three basic topologies based on single loop control are defined and investigated in more detail in the following. The topologies differ mainly in terms of feedback source and error estimation. The double edge PEDEC unit will be used throughout the investigations. Without loss of generality, it is assumed throughout the investigations, that the pulse levels in the controller are identical, i.e. $V_R = V_C = V_I$. The three topologies are shown in Fig. 5, Fig. 6 and Fig. 7 respectively.

PEDEC Voltage Feedback Control – Type 1 (VFC1)
PEDEC VFC1 is characterized by a voltage feedback from the switching power stage output v_p. The feedback path compensator is a simple attenuation, and the compensator block *C* is a linear filter. The topology is furthermore characterized by a *zero order reference shaping*, i.e. the reference shaping block *R* is completely omitted such that the error estimation is based on a direct comparison of input and output pulses. Despite the simple controller structure of PEDEC VFC1, the system introduces a powerful and flexible control of system performance.

PEDEC Voltage Feedback Control – type 2 (VFC2)
PEDEC VFC2 resembles PEDEC VFC1 in terms of feedback source. However, the topology differs by *first order reference shaping* in combination with a *matched first order output feedback shaping* in the A block. This also lead to different compensator characteristics (C).

PEDEC Voltage Feedback Control – type 2 (VFC3)
PEDEC VFC3 differs significantly from the other two topologies by utilizing *global* feedback from v_o, in combination with *second order reference shaping*

for optimal error estimation. Including the filter in the loop significantly changes the compensator characteristics.

The three topologies have been subjected to a detailed investigation in [12]. Loop shaping methods will be addressed by presenting a general frequency normalized loop synthesis methods. Following, illustrative case example will be synthesized and evaluated for each topology.

4.2 PEDEC VFC1 Case example

Despite the simplicity of the controller, the system enables powerful control of the performance of the switching power amplification stage. Note how the audio signal remains digital or pulse modulated throughout the main audio chain. No analog modulator or carrier generator is needed in the digital PMA system. The system is essentially controlled by the digital modulator.

Given the linear control function in (11), it is straightforward to derive the equivalent linear model of the system as shown in Fig. 8. The individual elements of the controller are also defined in the figure. The loop components are:

$$\begin{cases} C(s) = K_C \dfrac{(\tau_{z1}s+1)}{(\tau_{p1}s+1)(\tau_{p2}s+1)(\tau_{p3}s+1)} \\ B(s) = K_P k_{PEDEC} \\ A(s) = \dfrac{1}{K} \\ R(s) = 1 \end{cases} \tag{13}$$

The C compensator provides sufficient flexibility for loop optimization. The loop transfer function is:

$$L_1(s) = \frac{K_P k_{PEDEC} K_C}{K} \frac{(\tau_{z1}s+1)}{(\tau_{p1}s+1)(\tau_{p2}s+1)(\tau_{p3}s+1)} \tag{14}$$

The compensator gain K_C has to be tuned to realize the desired loop bandwidth. The linear model in Fig. 8 illustrates the *dual* input configuration, i.e. the system transfer function from v_r to v_p has two contributions:

$$\begin{aligned} H(s) &= \frac{C(s)B(s)}{1+A(s)C(s)B(s)} + \frac{K_P}{1+A(s)B(s)C(s)} \\ &= \frac{K_P[C(s)k_{PEDEC}+1]}{1+A(s)C(s)B(s)} \end{aligned} \tag{15}$$

In the special but not unusual case where $K = K_P$, the transfer function is *constant*:

$$H(s) = \frac{K[C(s)k_{PEDEC} + 1]}{1 + C(s)k_{PEDEC}} = K \tag{16}$$

This characteristics is significantly different from the previously analyzed control methods. The explanation is that PEDEC VFC1 is *only contributing to system performance as long as there are errors present.* In the general case, corresponding to $K \neq K_P$:

$$H(s) \approx \begin{cases} K & (f < f_u) \\ K_P & (f >> f_u) \end{cases} \tag{17}$$

$K \neq K_P$ can be viewed as a linear error that the PEDEC controller will attempt to correct for. Obviously, this correction is only possible within the bandwidth of the system. With a standard second order filter for demodulation:

$$F(s) = \frac{\omega_o^2}{s^2 + \frac{\omega_o}{Q_o}s + \omega_o^2} \tag{18}$$

The system transfer function will essentially be determined by the demodulation filter. A set of general system parameters in proposed below:

Parameter	Value	Comment
$k_{PEDEC} = \frac{2t_o}{t_s}$	$\frac{1}{5}$	Equivalent PEDEC unit gain.
$f_{p1} = \frac{1}{\tau_{p1}}$	$\frac{1}{20}f_u$	Loop parameter
$f_{p2} = \frac{1}{\tau_{p2}}$	f_{p1}	Loop parameter
$f_{p3} = \frac{1}{\tau_{p3}}$	$2f_u$	Loop parameter
$f_{z1} = \frac{1}{\tau_{z1}}$	$\frac{1}{2}f_u$	Loop parameter
f_o	2	Filter natural frequency
Q_o	$\frac{1}{\sqrt{3}}$	Filter Q

The specification of the PEDEC unit gain is based on an estimation of the necessary correction range, and the specified gain of 0.2 represents a good compromise. A higher k_{PEDEC} compromises the modulation index range with

optimal control and the lower gain on the other hand compromises the range of error size. This will especially be a problem in terms of the correction of large magnitude linear errors.

4.3 Example realization

Specification

A case example is considered for the full audio bandwidth with a system gain of $K = 20dB$ and an equivalent power stage gain of $K_P = 20dB$.

Synthesis

The synthesis is trivial with the defined general loop shaping procedure. The bandwidth of the considered case example is $f_u = 5$.

Verification

Fig. 9 shows Bode plots for each component in the loop and the resulting loop transfer function. The characteristics are much alike the VFC2 topology that was investigated in Chapter 6. The main difference is that the $C(s)$ compensator has to have a higher gain. Fig. 10 shows Bode plots for the individual components that contribute the closed loop system response. The following is verified:

- Within the bandwidth of the control system, the "feedthrough path" is suppressed, i.e. the system is controlled exclusively by the loop.
- Around the frequency of unity gain, both paths contribute to the system response such that the system gain remains constant.
- Beyond the bandwidth of the loop, the "feedthrough" path exclusively determines the system response.
- With a constant gain characteristic of PEDEC VFC1, the demodulation filter determines the system respnose.

Non-linear simulation

The system considered is again a 200W power stage, operating on a V_S power supply level. The parameters are:

Parameter	Value	Comment
f_B	20KHz	Bandwidth frequency
K	20dB	Amplifier gain
V_S	50V	Power supply rail
f_s	350KHz	$t_s = 2.86\mu s$
t_0	286ns	Realizes desired PEDEC unit gain
V_C, V_I, V_R	5V	Pulse amplitude levels.

There are quite a few differences between the linear feedback topologies presented in the previous chapter and a PEDEC controlled digital PMA. Some of the important differences are:

- The limited correction range.
- The dual input topology.
- The carrier frequency influences on e.g. stability.

PEDEC VFC1 has been subjected to a thorough low level simulation [12]. The essential results will be presented in the following. shows a simulation of the complete PEDEC VFC1 system at idle operation. This initial functional simulation of the system verifies that the correction system is stable and operating exactly as specified.

The capability to suppress pulse timing errors errors has been investigated by a parametric investigation of the near worst-case situation $M = 0.5$, $f = 5KHz$. Fig. 12 shows the PEDEC unit control signal and the resulting output in the two cases $t_d = 10ns$ and $t_d = 100ns$, respectively. It is very interesting to observe, how the controller applies anti-distortion with by widening the pulse when the error signal with a positive error signal during the positive going cycle and vice versa. The square wave error is recognized as the inverse blanking distortion, i.e. the control signal to the PEDEC unit *directly envisions the distortion type*. A general analysis provis that the improvement is constant and independent of t_d. In general, PEDEC VFC1 provides effective control over PTE errors and the performance improvements are easily controlled.
Pulse amplitude errors can have significant magnitude, especially if a simple non-stabilized power supply is used. The rejection of power supply perturbations is investigated by superposing the power rail with a 5KHz, 10Vpp harmonic perturbations. This causes an IM-distortion in the order of 5%-10%. Fig. 13 shows a simulation of the perturbed system with the PEDEC controller. The PEDEC controller compensates for the effect by widening the pulses (positive control signal v_e) where the PWM signal is compressed and vice versa. This is observed by looking at the control signal v_e.

An interesting characteristic of PEDEC control is that PEDEC will not oscillate in the traditional way at some unity gain frequency above the audio band, since the correction range is limited. Accordingly, the stability is limited and the effects thereof are equally limited (no tweeter burn out etc.). Another interesting aspect is the excellent transient response of the control system. This instant transient response is illustrated in Fig. 14.

5. Practical evaluation

Results presented in this paper will be based on a prototype developed in [13]. The modulator has been implemented on a dedicated SHARC processor based PCB. The power conversion stage was implemented on a very compact SMT PCB. Generally, the PEDEC controller is simple in implementation with a active and passive components. Thus, the controller only marginally influences the complexity of the system. A dedicated realization for a reduced 2KHz bandwidth (subwoofer/bass) is considered. PEDEC is investigated with a 200W power stage. The parameters for the implemented PEDEC digital PMA system are given below:

Parameter	Assignment
Resolution	8 bits
Bandwidth	2KHz
Carrier frequency	44.1KHz
Filter bandwidth	2KHz
Filter order	4
Supply rail	50V
System gain	26dB
Blanking delay t_d	80ns

The essense of PEDEC control is to *force equivalence* between the power stage output and the digital pulse with modulated (ideal) reference in all situations.

Fig. 15 shows the PMA output with f=500Kz and M=0.5 with a stabilized power supply. Fig. 16 shows the same situatiation with a non-stabilized power supply (10000μF). The intermodulation caused by power supply perturbations is significant, corresponding well with theory [12].

The PEDEC controller significantly reduces both THD and IM as shown in Fig. 17 where the output is investigated with the exactly same parameters set, only with PEDEC VFC1. Comparing the PEDEC controlled systems with the open loop system, the improvements are significant, about 20dB in distortion and 40dB in intermodulation (PSRR). It should be notedNote that the VFC2 topology performs somewhat better than VFC1, and is furthermore simpler in implementation. Thus, the digital PMA output with PEDEC VFC2 is very close to the reference performance.

Fig. 18 shows the output at M=0.1. The distortion improvement is 26dB resulting in 0.018% THD, verifying that the improvement in independent of output level. Fig. 19 shows the output at 1KHz, M=-20dB. The improvement in distortion is about 20dB as with the other topologies. A highly interesting aspect should be noted however. Clearly, the PEDEC controller *forces the*

output to resemble the shaped reference best possible. This leads to a phenomea that may be interpreted as *noise reshaping* [12], which leads to much improved noise characteristics – simplifying demodulation.

6. Conclusions

This papers has introduced PEDEC as a general method for enhanced power amplification of a pulse modulated signal. Three simple PEDEC based PMA topologies were proposed with different characteristics in terms of error estimation and feedback source. Loop shaping was addressed, and illustrated by example. Based on the detailed investigation in both time and frequency domain of the principle, PEDEC proved to realize a significantly reduced sensitivity to any error source existing in a switching power amplification stage. To complete the investigations, PEDEC has been evaluated in practice and shown to provide a much improved power amplification of the pulse modulated signal, forcing equivalence between the digital modulator output and the digital PMA power output. This dramatically simplifies high performance digital PMA design.

7. Patent Protection

PEDEC is protected by an international patent application [15]. Any interested partners are encouraged to contact Bang&Olufsen A/S (the author) for further information.

8. References

[1] Hawksford, M.O.J.
"Dynamic Model-Based Linearization of Quantized Pulse-Width Modulation for Applictions in Digital-to-Analog Conversion and Digital Power Amplifier Systems"
JAES. Vol.40. No.4. April 1992. pp. 235-252.

[2] Shajaan, M.
Digital PWM-forstærker til aktivt højttalersystem.
M.Sc. Thesis (in Danish).
Electronics Institute, Tech. Uni. of Denmark. 1992.

[3] Mellor, P.H. *et al.*
" Digital Sampling Process for Audio Class D Pulse Width Modulated Power Amplifiers" .
Electronic Letters. 2nd jan 1992. Vol.28. pp. 56-58.

[4] Craven, P.
" Toward the 24 bit DAC: Novel Noise-Shaping Topologies Incorporating Correction for the Nonlinearity in a PWM Output Stage"
JAES. Vol.41, No.5. 1993. pp. 291-313.

[5] R.E. Hiorns
"Digital Signal Processing and Circuit Design for Pulse Width Modulating Digital to Analouge Conversion "
Ph.D thesis. Kings College, University of London. 1994.

[6] Nielsen, Karsten
" Parallel Phase Shifted Carrier Pulse Width Modulation (PSCPWM) – A novel approach to switching power amplifier design "
102nd AES Convention. Munich, March 1997.
Preprint 4447 (26 pages)

[7] Nielsen, Karsten
" A Review and Comparison of Pulse Width Modulation methods for analog and digital input switching power amplifier systems "
102nd AES Convention. Munich, March 1997.
Preprint 4446 (57 pages).

[8] Nielsen, Karsten
" Pulse Edge Delay Error Correction – A Novel Power Stage Error Correction Principle For Power Digital – Analog Conversion "
103nd AES Convention. New York, USA. September 1997.
Preprint 4602 (47 pages).

[9] Nielsen, Karsten
"High Fidelity PWM based Amplifier Concept for active speaker systems with a very Low Energy Consumption"

Journal of the Audio Engineering Society.
July/August 1997. pp. 554-570.

[10] Nielsen, Karsten, Taul, Thomas, Andersen, Michael
" A comparison of Linear and Non-Linear Control Methods for Power Stage Error Correction in Switching Power Amplifiers "
104th AES Convention. Amsterdam, Holland. (43 pages).

[11] Risbo, Lars, Mørch, Thomas
" Performance of an all digital power amplification system "
104th AES Convention. Amsterdam, Holland.

[12] Nielsen, Karsten
" Audio Power Amplifier Techniques with Energy Efficient Power Conversion ".
Ph.D. Thesis.
Department of Applied Electronics, DTU, Denmark. May 1998.

[13] Neesgaard, Claus
" PEDEC based digital Pulse Modulation Amplifiers "
M.Sc. Thesis (in Danish).
Department of Applied Electronics, DTU, Denmark. 1998.

[14] Nielsen, Karsten
" PEDEC - A Novel Pulse Referenced Control Method for High Quality Digital PWM Switching Power Amplification "
IEEE Power Electronics Specialist Conference (PESC).
Japan, May 1998.

[15] Nielsen, Karsten.
" Pulse Referenced Control Method For Enhanced Power Amplification of a Pulse Modulated Signal "
International Patent Application.
Applicant: Bang&Olufsen A/S, Denmark

[16] Nielsen, Karsten
" Linearity and Efficiency performance of Switching Audio Power Amplifier Output Stages – A Fundamental Analysis "
105th AES Convention. San Francisco. September, 1998.

[17] Nielsen, Karsten
" MECC – A Novel Power Stage Error Correction Principle for High End Switching Power Amplification "
105th AES Convention. San Francisco. September, 1998.

[18] Frederiksen, Thomas, Christensen, Frank and Nielsen, Karsten
" Paralleled Phase Shifted Carrier Pulse Width Modulation (PSCPWM) Schemes - A Fundamental Analysis.
106th AES Convention. Munchen, Germany. May 1998.

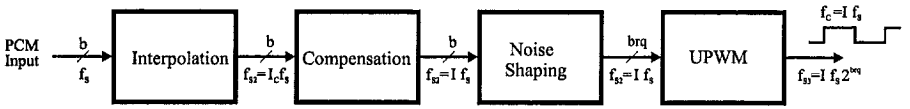

Fig. 1 Digital PCM–UPWM modulator using precompensation

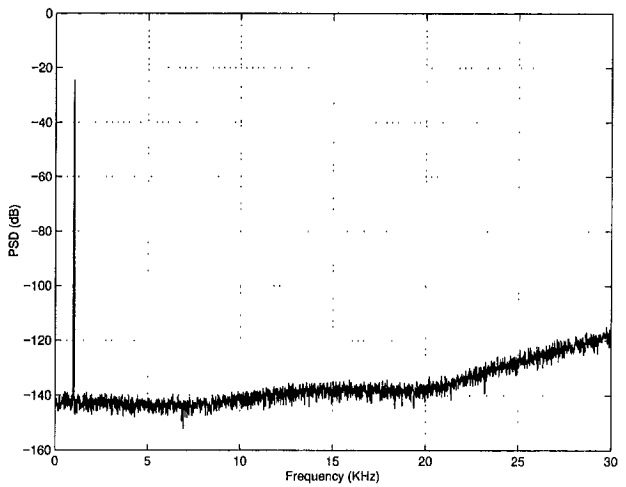

Fig. 2 Simulation of digital LPWM modulator output PSD (1KHZ, M=0.1). 16K samples are used in the FFT. THD<0.0001%.

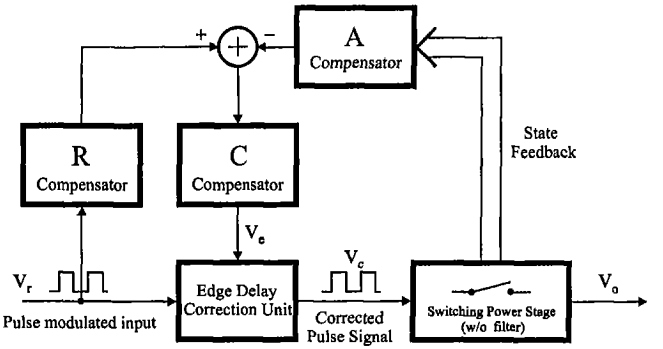

Fig. 3 The general elements of a PEDEC controller.

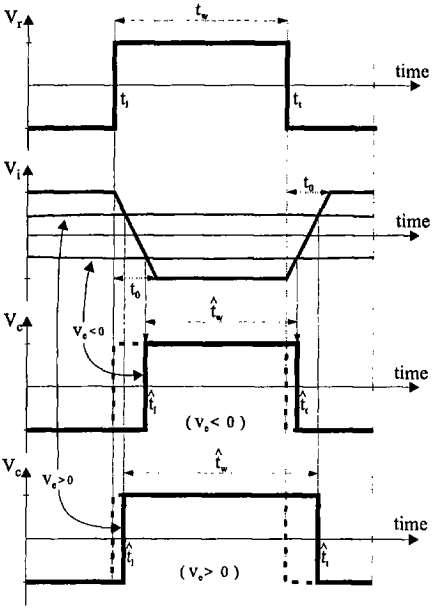

Fig. 4 Proposed realization of a linear double edge PEDEC control function.

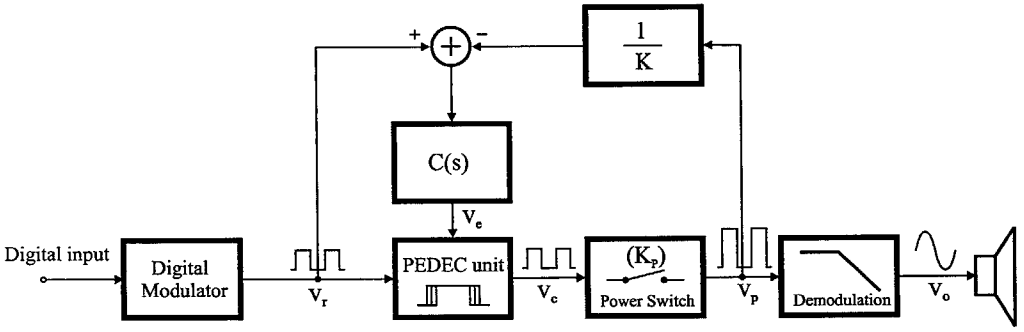

Fig. 5 PEDEC VFC1 Topology.

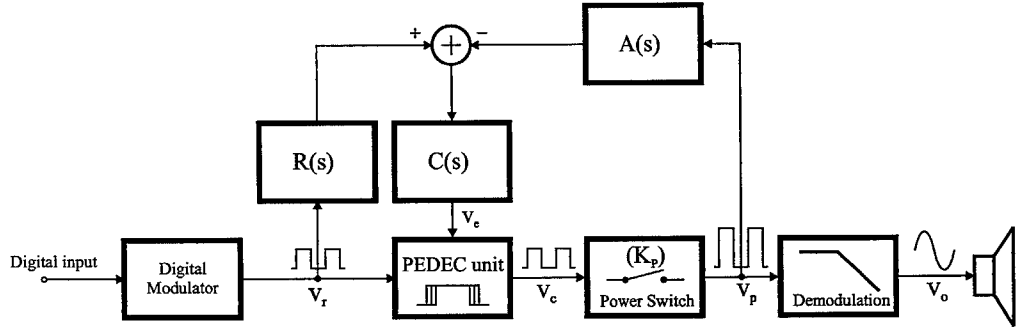

Fig. 6 PEDEC VFC2 Topology.

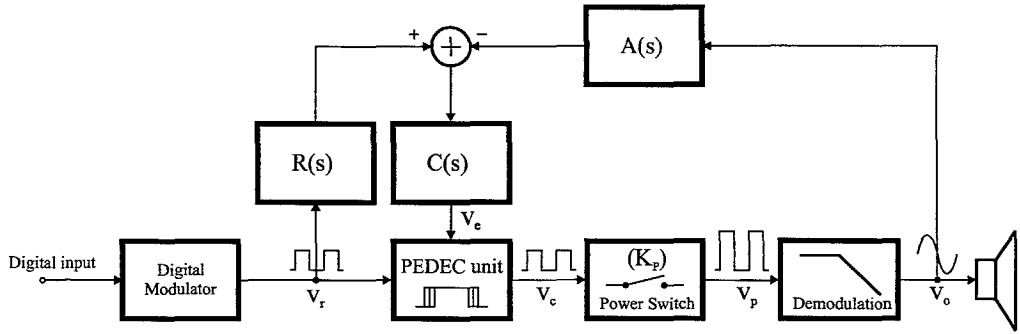

Fig. 7 PEDEC VFC3 Topology.

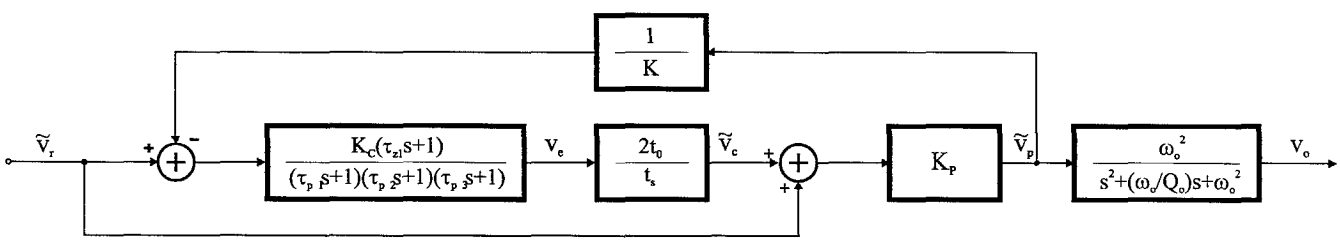

Fig. 8 Dual input linear model of PEDEC VFC1 Topology with all compensator elements defined.

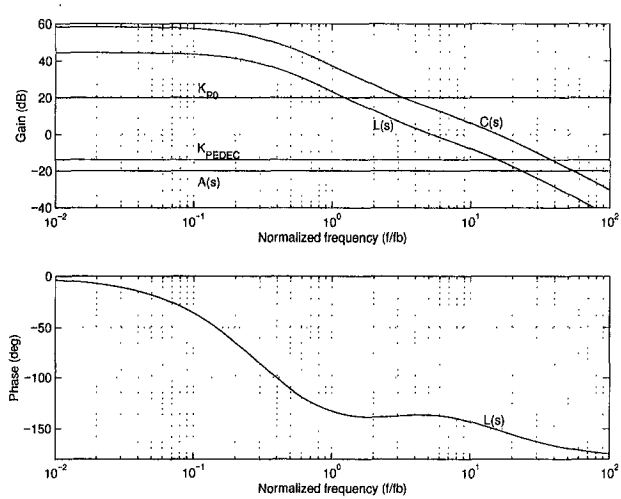

Fig. 9 Loop components and the resulting loop transfer function for PEDEC VFC1.

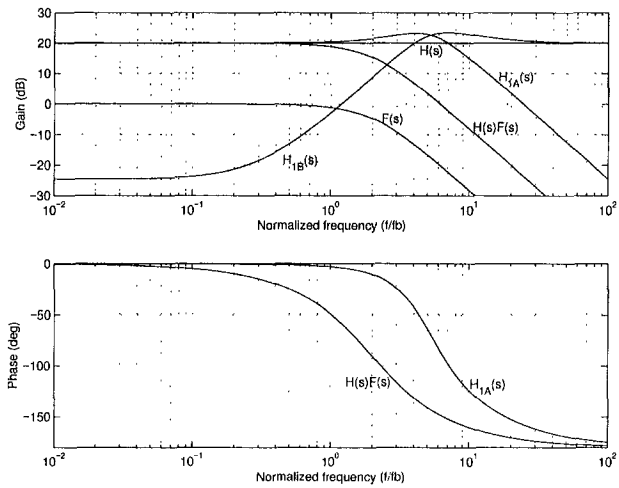

Fig. 10 Contributions to the system transfer function for PEDEC VFC1.

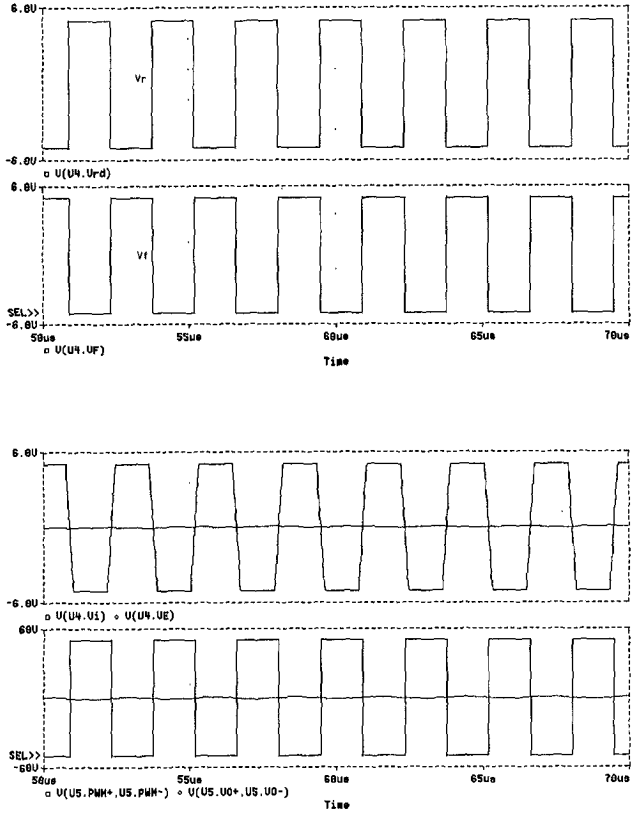

Fig. 11 Functional simulation of PEDEC VFC1 system. Reference input v_r and feedback v_f, PEDEC unit signals v_e, v_i and finally the resulting corrected power stage output.

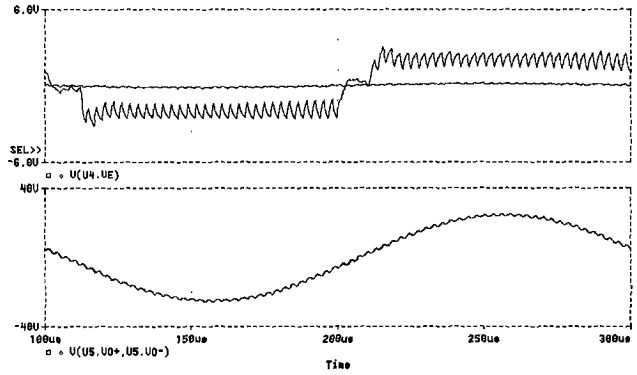

Fig. 12 PTE correction for PEDEC VFC1. *M≈0.5. f=5KHz.* Top – v_e with t_D=*10ns* and t_D=*100ns.* v_e clearly envisions the distortion type. Bottom – Resulting output. Even large linear and non-linear errors are corrected effectively by the PEDEC controller.

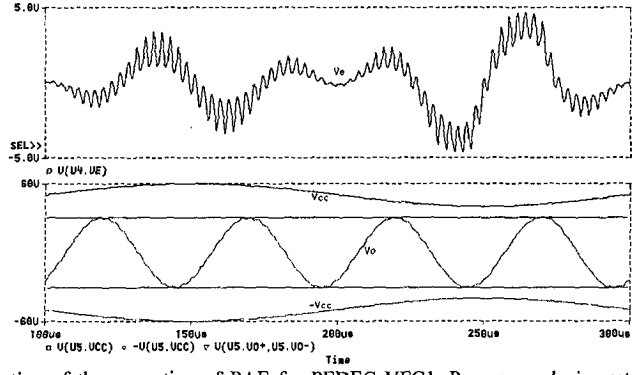

Fig. 13 Simulation of the correction of PAE for PEDEC VFC1. Power supply is perturbed with a 5KHZ, 10Vpp error signal. *M=0.5. f = 20KHz* (worst-case). The PEDEC controller effectively reduces the intermodulation and improves PSRR by about 25dB corresponding to theory.

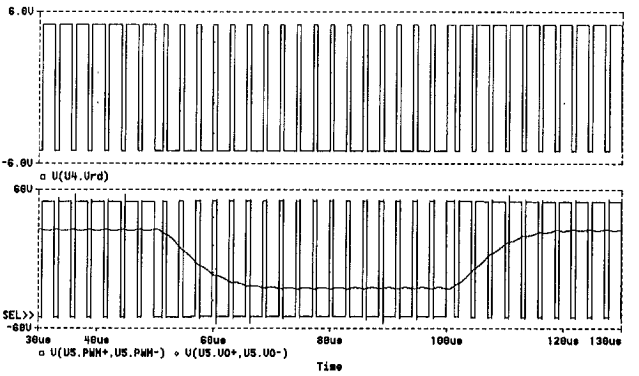

Fig. 14 A simulation of the excellent transient response characteristics of PEDEC VFC1. Close investigation of the pulse output v_p shows exact and *instant* amplification of the reference. The explanation is that PEDEC VFC1 only "works" when errors are generated, and does not affect the amplification otherwise.

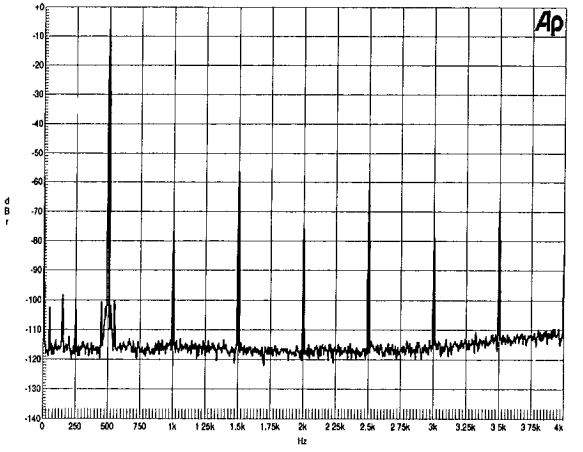

Fig. 15 Non-controlled output at f=500Hz, M=0.5. **Stabilized** power supply. The distortion is caused primarily by a blanking delay of 80ns.

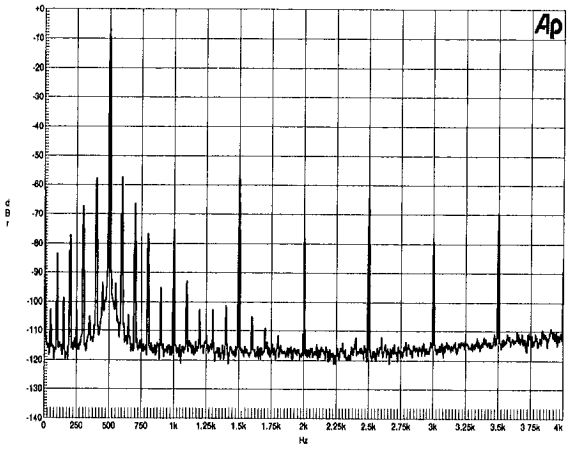

Fig. 16 Non-controlled output at f=500Hz and M=0.5. **NON-stabilized** supply (10000μF). Note the severe intermodulation distortion.

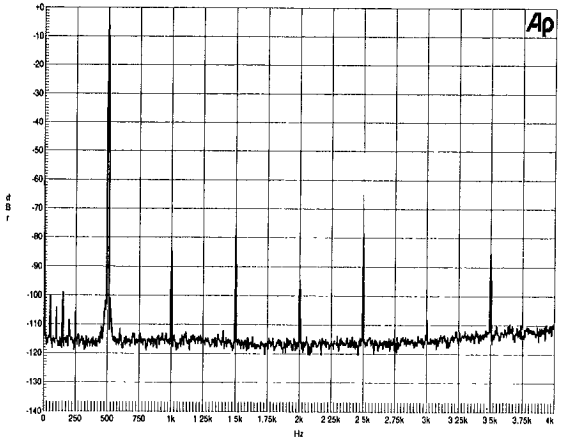

Fig. 17 PEDEC VFC1. 500Hz and M=0.5. **NON**-stabilized power supply. Comparing with the open loop system, PSRR is improved 40dB and THD 20dB with PEDEC VFC1.

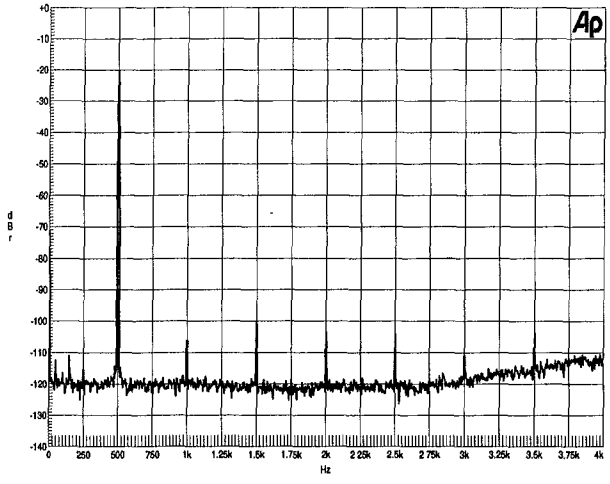

Fig. 18 PEDEC VFC1. 500Hz, M=0.1 **NON-stabilized** supply. The improvement in THD is 26dB leading to THD=0.018%.

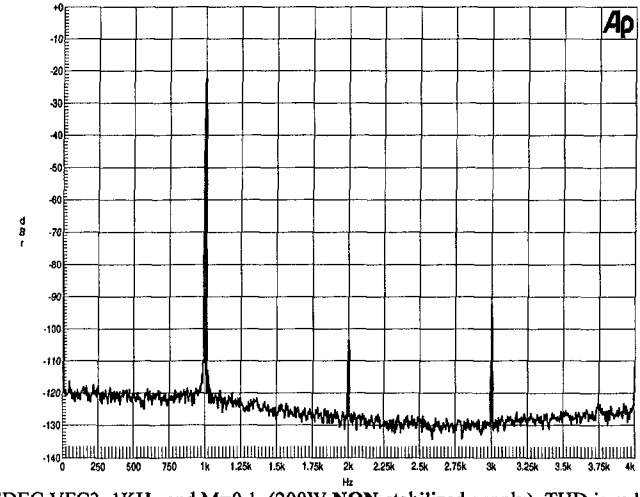

Fig. 19 PEDEC VFC3. 1KHz and M=0.1. (200W **NON**-stabilized supply). THD is reduced 20dB and PSRR is reduced approximately 40dB. Note the significantly changed noise floor characteristic. The loop modifies the output to resemble the second order shaped reference best possible. This leads to noise "reshaping" by the PEDEC VFC3 system.